Transistor → CPU → GPU → Model → Agent → Society → Autonomic Systems → Objective Layer → Co-Designed Matter → Embodied Mesh

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This paper follows a single thread: how computation climbs an abstraction ladder where each rung packages the mess beneath it and spends that simplicity on a larger competence above it. We start with the transistor, a reliable bit switch that made digital logic composable. The CPU turned bits into instructions; the GPU turned instructions into parallel tensor throughput; models turned tensors into learned capabilities. From there, we project forward: agents that pursue goals with tools, societies of agents coordinated by incentives, autonomic systems that manage themselves against service-level objectives, an objective layer that binds action to proofs and rights, co-designed matter where models emit manufacturable artifacts, and, finally, an embodied mesh—ubiquitous, resilient computation woven into the world. Our aim is neither hype nor nostalgia. We propose crisp primitives, abstractions, enabling mechanisms, and measurable guarantees for each rung, along with the failure modes and guardrails that keep sophistication from collapsing into fragility. The result is a roadmap for researchers and builders: what to standardize, what to measure, and where co-design pressure flows next. If the ladder holds, capabilities compound; if it snaps, complexity recurses into brittleness. We show how to climb deliberately.

Keywords: transistor, CPU, GPU, deep learning model, AI agent, multi-agent systems, autonomic computing, verifiable computing, objective layer, proof-carrying code, inverse design, chiplets, embodied AI, edge computing, systems co-design, incentives, SLOs, reliability, governance, energy.

Note: In the Epilogue, GPT-5 discusses the plight of humanity during these transitions and those responsible for this vision. 53 pages. CC4.0.

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1. Transistor: Reliable Bits and the Discipline of Digital

1.1 CMOS as the low-leakage switching primitive

- **Why CMOS won:** Complementary devices (nMOS pull-down, pMOS pull-up) yield near-zero static current in steady logic 0/1, so average power is dominated by charging/discharging capacitances.
- **Inverter as the canonical gate:** One pMOS in series with VDD and one nMOS to GND. Transfer curve gives noise margins; sizing sets switching threshold near VDD/2.
- **First-order device laws (for reasoning, not sign-off):**
    - Strong-inversion Id (long-channel):
      Id_sat ≈ (1/2) * mu_n * C_ox * (W/L) * (Vgs - Vth)^2
    - Subthreshold leakage (Vgs < Vth):
      I_sub ≈ I0 * exp((Vgs - Vth)/(n*Vt)) with Vt = kT/q
    - Dynamic switching energy per transition: E_sw ≈ C_load * V^2
    - Dynamic power at activity factor alpha and clock f: P_dyn ≈ alpha * C_total * V^2 * f
- **Leakage channels that matter at scale:** subthreshold, gate-oxide tunneling, junction BTBT. As Vth is lowered or T rises, I_sub grows exponentially.
- **Modern device knobs:** high-k/metal-gate, strain engineering, FinFET → GAA nanosheets to keep electrostatic control as L shrinks; multi-Vt libraries to trade speed vs leakage.

Discipline gained: a switch that is almost lossless at rest and predictably lossy only when toggling. This makes logic composable and enables the “counting” mentality of digital systems.

1.2 From devices to standard cells: design rules, PnR, timing

- **Design rules (DRC) as a contract with the fab:** min width/spacing, enclosure/overlap, via arrays, density windows. At advanced nodes add multi-patterning/EUV constraints and forbidden pitch rules. DRC/LVS closure is step zero for “reliable bits.”
- **Standard-cell libraries:** NAND/NOR/inverter flops with multiple drive strengths (X1, X2, …) and threshold options (HVT/SVT/LVT). Logical effort gives quick delay vs size tradeoffs; leakage bins give power-speed trade space.
- **Physical synthesis & PnR flow:**

1. Floorplan & power grid (IR-drop/EM budgets).
2. Placement (minimize wirelength/congestion).
3. Clock-tree synthesis (skew/jitter budgets).
4. Global/detail routing (respect blockages, DRC).
5. Parasitic extraction (R,C; sometimes Cc).
6. Timing closure with ECO loops (resize/buffer/repower/retime).

- **Static timing analysis (STA):** checks setup/hold across PVT corners (process, voltage, temperature). Corners catch worst-case delay and best-case races. On-chip variation (OCV/AOCV/POCV) models local randomness; sign-off adds derates and margins.
- **Signal integrity & reliability:** crosstalk delay/noise, ground bounce, IR-drop, electromigration. Fixes include shielding, spacing, wider metals, more vias, decaps, dynamic deskew.
- **DFM & yield:** redundant vias, pattern matching, metal fill for density, hotspot avoidance. The cell-level discipline scales bits to millions/billions of synchronized toggles without falling apart.

Discipline gained: a repeatable, tool-driven pipeline that turns Boolean intent into a manufacturable, timed, and verifiable fabric.

1.3 Power, thermal, and the end of Dennard: limits that shape layers above

- **Dennard scaling premise (constant-field):** feature size -> 1/S, supply V -> 1/S, frequency -> S, C -> 1/S, so P_gate ≈ C*V^2*f stays ~constant and power density stays flat.
- **Why it broke:** VDD could not keep dropping proportionally (noise margins, Vth limits, variability), but f and device count kept rising. Consequences:
    - **Power wall:** P ≈ alpha*C*V^2*f grows; leakage becomes non-trivial as Vth falls.
    - **Thermal wall:** hot spots dominate; TDP caps force guard-bands.
    - **Dark silicon:** not all transistors can be on simultaneously at rated frequency.
    - **Interconnect wall:** RC delay and energy to move data (not compute) becomes first order.

- **Architectural responses:**
    - **Multicore vs. frequency:** harvest throughput at lower per-core f and V.
    - **Specialization:** fixed-function or semi-programmable datapaths (SIMD, tensor cores) for higher ops/J.
    - **Memory hierarchy emphasis:** bigger SRAMs, HBM stacks, on-package fabrics to cut joules/bit-moved.
    - **DVFS, power gating, body bias:** dynamic control to stay under thermal envelopes.
- **Variability & margins:** random dopant fluctuations, line-edge roughness, device aging (BTI, HCI) push larger timing/power guard-bands; adaptive voltage/frequency scaling and error-detecting flops (Razor-style) claw back margin when safe.
- **Implications upward:**
    - **CPU design:** leaner, wider at lower clocks; favor IPC gains that don't spike power; prioritize cache efficiency.
    - **GPU design:** massive parallelism but constrained by memory BW/energy; push lower precision (FP8/INT8).
    - **Model design:** quantization, sparsity, operator fusion to reduce data motion; training/inference schedules co-designed with memory fabrics.

Discipline gained: power and heat are first-class specs. Every higher layer (CPU, GPU, model) must treat joules/bit and joules/op as budgeted resources, not afterthoughts.

Section takeaway: CMOS gives us a nearly ideal digital switch; cell-based design and PnR make billions of them tractable; but post-Dennard, power/thermal and interconnect physics set hard budgets that shape everything built above.

2. CPU: Instructions, Memory, and General-Purpose Control

2.1 ISA, pipelines, speculation, caches: hiding latency behind structure

- **ISA as contract:** visible ops, registers, memory model, and calling/ABI (e.g., x86-64, ARMv8, RISC-V). Microarchitectures freely translate ISA ops → µops (decode/rename) while preserving the contract.

- **Pipelines:** fetch → decode → rename → dispatch → issue → execute → writeback → retire. Depth increases frequency but raises branch/mem mispredict cost.
- **Out-of-order + speculation:** large issue queues, register renaming, and reorder buffers exploit instruction-level parallelism (ILP). Branch predictors (TAGE, perceptron, neural hybrids) and speculative loads hide control/memory latency; mispredictions flush.
- **CPI accounting:** CPI ≈ CPI_base + CPI_branch + CPI_mem + CPI_sync. Aim to keep CPI near 1 despite stalls.
- **Caches (latency hierarchy):** private L1I/L1D → L2 → shared LLC. Average Memory Access Time: AMAT = L1_hit + (L1_miss × L2_penalty) + …; prefetchers convert predictable miss streams into hits; non-blocking caches allow MLP (memory-level parallelism).
- **Coherence & consistency:** MESI/MOESI directories keep shared data coherent; memory models (TSO, RC) plus fences define legal reorderings—vital for correct multicore code.

Discipline gained: predictable single-thread latency via deep microarchitectural tricks that the ISA abstracts away.

2.2 Virtual memory, protection, and process abstraction

- **Address virtualization:** per-process virtual address spaces map via page tables; TLBs cache translations; huge pages (e.g., 2 MiB/1 GiB) trade fragmentation for fewer TLB misses.
- **Protection rings & privilege:** user vs kernel modes, page permissions (R/W/X), W^X policies, ASLR. Syscalls are the controlled gateway to devices and the kernel.
- **Isolation & sharing:** copy-on-write, memory-mapped files, shared anonymous pages, IPC primitives. NUMA awareness binds threads/memory to local controllers to avoid cross-socket penalties.
- **Virtualization & enclaves:** hypervisors (VT-x/AMD-V) multiplex hardware; nested paging (EPT/NPT) preserves performance. TEEs (e.g., SGX/SEV) add attested isolation for secrets.
- **Security after Spectre/Meltdown:** speculation barriers, constant-time coding, and microcode/firmware mitigations integrate with the VM/protection story.

Discipline gained: a safe, multiplexed machine image—processes feel alone while sharing hardware at scale.

2.3 Diminishing ILP and the multicore era: what still belongs on CPUs

- **Why ILP stalled:** deeper pipelines hit branch limits; wire delays and power walls cap frequency; OoO windows face quadratic energy/area growth; memory latency improved far slower than clocks.
- **Amdahl/Gustafson tension:** even modest serial fractions cap speedup; strong scaling demands lower-latency cores for the sequential tail, not just more cores.
- **Multicore/Heterogeneous response:** many moderate cores + SIMD/crypto/AI extensions (AVX-512, SVE, SHA/AES) under a power cap; offload dense kernels to GPUs/ASICs; keep orchestration local.
- **What the CPU is still best at:**
    - **Latency-critical control:** OS scheduling, interrupts, RPC endpoints, coordination loops.
    - **Branchy/irregular code:** parsers, graph traversals, JITs, SMT/SAT search with frequent backtracking.
    - **Mixed I/O & syscalls:** storage/network stacks, compression, encryption with data-dependent control.
    - **Small-batch / low-tail inference:** tiny models, request-per-core with strict p99 SLOs.
    - **Safety & orchestration:** transactions, consensus participants, watchdogs, exception handling.
- **Design emphases going forward:** big-little (performance + efficiency cores), fast wake/sleep, rich prefetch + run-ahead for pointer-chasing, cache QoS, better HW queues/atomics, and tighter NIC/SSD coupling (DPUs/SmartNICs) with low-overhead syscalls.
- **Programmer's heuristic:** if work is **control-heavy, latency-sensitive, or highly irregular**, keep it on CPUs; if it's **dense numeric with high arithmetic intensity**, push down the ladder (GPU/ASIC).

Discipline gained: CPUs remain the sovereignty layer—fast decisions, protection, and orchestration—while bulk math migrates to throughput engines below.

3. GPU: Throughput Machines for Parallel Tensors

3.1 SIMT, warps/wavefronts, shared memory, tiling

- **SIMT mental model:** one kernel, many threads; hardware issues instructions to a **warp/wavefront** (e.g., 32 or 64 threads) in lockstep. The unit of scheduling is the warp, not the thread.
    - **Latency hiding:** keep many warps resident per SM/CU so others run while one waits on memory.
    - **Occupancy (rule-of-thumb):** occupancy = active_warps_per_SM / max_warps_per_SM; adequate but not maximal occupancy is usually enough if you are bandwidth- or compute-bound elsewhere.
- **Memory coalescing:** consecutive threads should touch consecutive addresses.
    - Bad: A[tid * stride] with large stride.
    - Good: A[base + tid] and tile/block striding.
- **Shared memory (SMEM):** low-latency, programmer-managed cache.
    - **Use:** stage tiles from global memory, perform reuse-heavy math (GEMM/conv), then write back.
    - **Bank conflicts:** arrange layouts so thread i hits bank i; pad dimensions when necessary.
- **Register pressure:** more registers per thread → fewer resident warps → possible throughput loss. Tune tile sizes to stay below register spill thresholds.
- **Tiling (blocking):** split problem into tiles that fit registers/SMEM to maximize reuse.
    - **2D/3D tiles:** common for GEMM/conv/attention.
    - **Double-buffering:** overlap global→SMEM loads with compute using asynchronous copy and barriers.
- **Warp-level collectives:** shuffles, ballots, reductions avoid SMEM round-trips for small exchanges.
- **Sync primitives:** prefer warp-scope ops; use __syncthreads()/barriers only when truly needed.

Checklist: coalesced loads, tile for reuse, avoid bank conflicts, watch register count, keep enough active warps to hide memory latency.

3.2 Tensor/matrix engines, HBM, interconnect topologies

- **Tensor/matrix engines:** fixed-function units that accelerate small matrix multiply–accumulate (MMA) tiles (e.g., 16x16xK).
    - **Programming paths:** WMMA/Tensor Core intrinsics, vendor libraries (cuBLASLt, CUTLASS, rocBLAS, etc.).
    - **Precision ladder:** FP32 → TF32/BF16/FP16 → FP8/INT8. Lower precision boosts FLOPs/J if numerics permit (use mixed-precision accumulators and loss-scaling/FP8-aware training).
    - **Operator fusion:** fuse pointwise ops around GEMMs (bias, activation, dropout) to reduce memory traffic.
- **Roofline framing:** achieved_flops <= min(peak_flops, operational_intensity * mem_bandwidth).
    - **operational_intensity (OI):** flops_per_byte_moved. Raise OI via tiling/reuse/fusion.
- **HBM stacks:** very high bandwidth, moderate latency.
    - **Implication:** design kernels that convert bandwidth into OI; avoid tiny, random accesses that defeat burst transfers.
- **On-package & node interconnects:**
    - **Intra-node:** NVLink/NVSwitch, Infinity Fabric, PCIe. Bandwidth and topology determine how well tensor-parallel/pipeline-parallel jobs scale.
    - **Inter-node:** fat-tree, dragonfly, torus; collective performance (all-reduce/all-to-all) gates large-model training.
    - **Collectives libraries:** NCCL/RCCL/oneCCL; pick parallelism strategy (data/model/tensor/pipeline) to match your fabric.
- **Memory hierarchy on GPUs:** large register files → SMEM/L1 → L2 → HBM.
    - Aim for high L2 hit rates; prefetch or stage via SMEM; prefer strided patterns that map to cache lines.

Checklist: target tensor cores with the right datatypes, raise OI with tiling/fusion, match parallelism to your interconnect's strengths, watch collective time in profiles.

3.3 When GPUs win (and lose): divergence, locality, bandwidth walls

- **GPUs win when…**
    1. **High arithmetic intensity:** OI is large (e.g., dense GEMM/conv/attention).
    2. **Regular parallelism:** many identical threads with predictable memory access.
    3. **Large batches/tiles:** enough work per kernel to amortize launches and saturate SMs.
    4. **Amenable precision:** can drop to BF16/FP16/FP8/INT8 without accuracy loss.
    5. **Collectives-friendly:** training layouts that minimize all-reduce or align with topology.
- **GPUs struggle when…**
    1. **Divergence:** threads in a warp take different branches; effective throughput ~= average active lanes. Mitigate with data reordering, predication, warp-specialization.
    2. **Irregular sparsity/graphs:** pointer chasing, hash tables, dynamic work queues; consider CPU or specialized sparse kernels and reordering to improve locality.
    3. **Tiny problems or microbatches:** underfill SMs; fuse ops or batch requests.
    4. **Bandwidth wall:** kernels with low OI are memory-bound; focus on reuse, compression, quantization, and fused epilogues.
    5. **Collective-heavy scaling:** all-to-all/mixture-of-experts or large tensor-parallel can bottleneck on fabric; reconsider partitioning or topology-aware placement.
    6. **Tight latency SLOs with control flow:** RPC endpoints, parsing, crypto with data-dependent branching—keep on CPUs or use small on-die accelerators.
- **Profiling signals to watch (vendor tools):**
    - **sm_efficiency / alu_utilization:** how busy compute units are.
    - **achieved_occupancy:** resident warps vs maximum.
    - **dram_utilization, l2_hit_rate, bytes/FLOP:** memory-bound vs compute-bound.
    - **warp_execution_efficiency, branch_efficiency:** divergence.
    - **shared_transactions_per_request:** bank conflicts.

    - **time_in_collectives:** scaling wall indicator.

- **Tactics to move the needle:**
    - **Make it regular:** reorder data, block-sparse to semi-structured, bucket by shape/length.
    - **Raise OI:** larger tiles, re-computation vs writes (checkpointing), fuse ops.
    - **Reduce bytes:** quantize, pack, use layout transformations (e.g., NHWC/row-major for coalescing).
    - **Pipeline:** overlap copy and compute (async memcpy + barriers), double-buffer SMEM.
    - **Right-size kernels:** autotune tile sizes vs registers/SMEM to avoid spills and keep occupancy "enough."

Section takeaway: GPUs are throughput engines: maximize parallel regular work, feed tensor cores with the right tiles and dtypes, and fight the bandwidth wall with locality, fusion, and topology-aware scaling. When the workload refuses to be regular or large enough, keep the CPU in charge—or reach for a domain-specific accelerator.

4. Model: Differentiable Programs and Scaling Laws

4.1 Computation graphs, autograd, kernels, and compilers

- **Graph as program:** A model is a DAG of tensor ops; edges carry shapes/dtypes; nodes carry params and state (e.g., BN stats, RMSNorm scale). Training = forward pass (compute loss) + reverse pass (backprop on the same graph).
- **Autograd mechanics:**
    - For op y = f(x, w), autograd stores minimal *ctx* to compute local Jacobian-vector products on the backward sweep.
    - Memory vs recompute: checkpoint subgraphs so backward recomputes their forward (trade FLOPs for RAM).
    - Mixed precision: keep a *master FP32* copy of weights; cast forward/backward to BF16/FP16/FP8; use loss scaling to avoid underflow.

- **Kernels:** High-traffic ops dominate time/energy (GEMM, conv, attention, normalization, softmax, elementwise). Aim for operator fusion (e.g., GEMM+bias+activation+dropout) to raise arithmetic intensity and cut memory traffic.
- **Dataflow compilers:** XLA, TorchInductor, TVM, IREE, and Triton lower graphs to device kernels with tiling, vectorization, and layout selection.
    - **Canonical passes:** CSE, algebraic simplification, shape specialization, fusion, scheduling, memory planning.
    - **Numerics-aware lowering:** choose dtypes per edge, keep accumulators in higher precision; enable kernel epilogues to avoid extra reads/writes.
- **Attention-specific tricks:** FlashAttention/variants compute softmax(attn) with blockwise IO to avoid materializing NxN score matrices; causal masking and KV tiling preserve locality; paged KV cache for long contexts at inference.

Checklist: define graph cleanly, fuse hot paths, checkpoint long spans, cast precisely (master FP32, compute BF16/FP16/FP8 with safe accumulators), and inspect compiler IR for missed fusions.

4.2 Data/parameter parallelism, sharding, quantization, sparsity

- **Parallelism taxonomy (training):**
    - **Data parallel (DP):** replicate model on N devices, split batch; all-reduce grads each step. Simple; comms scale with param size.
    - **Tensor/model parallel (TP):** shard large matrices across devices (e.g., column/row parallel GEMMs). Reduces per-device memory; adds intra-layer comms.
    - **Pipeline parallel (PP):** split layers into stages; microbatch to keep stages busy; bubble overhead minimized by enough microbatches.
    - **Hybrids:** DP x TP x PP; add **sequence/context parallel** (shard sequence dimension) to shrink activation memory; **optimizer sharding** (e.g., ZeRO) to partition states.
- **State accounting (per device, rough order):**
    - Params: P bytes; Optimizer: ~2P (Adam moments); Gradients: P; Activations: A(batch, seq, width, depth).

    - ZeRO-1/2/3 progressively shard optimizer, grads, then params, reducing O(P) per device.

- **Quantization (train & infer):**
    - **Training:** BF16 as default; FP8 emerging with FP16/BF16 accumulators; stochastic rounding helps.
    - **Inference:** INT8/INT4/ternary; per-tensor vs per-channel scales; symmetric vs affine; quantization-aware training or post-training calibration (e.g., percentile/entropy).
    - **KV cache compression:** quantize KV to 8/4-bit; grouped scales maintain quality.
- **Sparsity:**
    - **Structured:** N:M sparsity (e.g., 2:4) maps to hardware-friendly kernels.
    - **Unstructured:** prune small-magnitude weights; needs sparse kernels and reordering to win.
    - **Activation sparsity:** ReLU/gated units; runtime skipping.
    - **MoE (Mixture-of-Experts):** route tokens to k of E experts; increases parameter count without proportional FLOPs; heavy all-to-all traffic—place experts/topology carefully.
- **Sharding layouts that work in practice:**
    - Attention: shard heads or the hidden dimension (column-parallel QKV, row-parallel output).
    - MLP: column-parallel first GEMM, row-parallel second; fuse bias+activation+dropout.
    - Use topology-aware placement (NVSwitch islands; minimize cross-chassis traffic).

Checklist: pick DP/TP/PP such that per-device memory fits with headroom; use ZeRO or equivalent; quantize where tolerant; prefer structured sparsity or MoE only when fabric can sustain all-to-all.

4.3 Evaluation beyond accuracy: robustness, calibration, efficiency

- **Accuracy is not enough:** report task scores *and* operational properties. Establish a minimal “vitals panel” per model family.

- **Robustness:**
    - **Distribution shift:** evaluate on out-of-domain and long-tail subsets; track relative drop vs IID.
    - **Adversarial/perturbation tests:** small input corruptions, prompt/wording variants, noise, compression; report worst-case within a budget.
    - **Safety/guardrails:** jailbreak resistance, refusal correctness, harmful content filters—measure false accept/false reject.
- **Calibration:**
    - **Reliability diagrams, ECE (expected calibration error):** bin by confidence, compare accuracy vs confidence; lower ECE is better.
    - **Brier score / NLL:** penalize overconfident errors; compare temperature scaling or Dirichlet calibration.
    - **Selective prediction:** coverage vs risk curves when the model can abstain.
- **Controllability & consistency:**
    - **Spec adherence:** task-SLA satisfaction under constraints (time, cost, safety).
    - **Self-consistency:** agreement across samples/temperatures; majority-vote accuracy; variance as instability proxy.
    - **Tool correctness:** for tool-using models, verify API argument validity and side-effect logs.
- **Efficiency metrics (train & infer):**
    - **Throughput:** tokens/s (train), requests/s (infer).
    - **Latency:** p50/p95/p99 end-to-end; cold vs warm; with/without batching.
    - **Cost:** $/1M tokens (train/infer), $/SLA-compliant task; amortize over utilization.
    - **Energy:** joules/token, watts @ TDP, datacenter PUE impact.
    - **Memory footprint:** params, optimizer state, activations, KV cache size vs context length.
    - **Utilization:** SM/TC occupancy, bytes/FLOP, all-reduce/all-to-all time fraction.
- **Reproducibility & variance:** seed control; report mean±sd across runs/checkpoints; include hardware/fabric details, compiler versions, fused-kernel choices, and dtype.

- **Deployment readiness:**
    - **Guarded decoding:** logit filters, safety constraints, content classifiers.
    - **Caching & chunking:** retrieve-augmented pipelines, KV reuse, speculative decoding; measure quality vs speed trade.
    - **Observability:** traces with per-op timing, OOM counters, numerical overflow/NaN sentinels.

Checklist: publish a compact scorecard: task metrics, OOD robustness, ECE/Brier, tokens/J and $/1M tok, p95 latency at target batch, KV footprint at max context, and fraction of time in collectives. Include ablations that show which fusions/quantizations matter.

Section takeaway: Treat models as compiled differentiable programs running on bandwidth-limited machines. Win by (1) expressing the graph so compilers can fuse and tile, (2) picking a parallelism/sharding mix that fits memory and fabric, (3) reducing bytes with quantization/sparsity without breaking numerics, and (4) reporting robustness, calibration, and efficiency—not just headline accuracy.

5. Agent: Goals, Tools, and Budgeted Autonomy

5.1 Policies with memory; planners, verifiers, and sandboxes

- **Memory model (what the agent can "know" and retain):**
    - **Ephemeral scratchpad:** step-local notes, chain-of-thought *structures* (plans, tables) without storing sensitive raw text.
    - **Session memory:** task context, partial results, open loops, per-tool rate limits.
    - **Long-term store:** schemas for facts, skills, and playbooks; TTLs, provenance, and redaction rules.
    - **Retrieval policy:** queries must include purpose + scope; deny-list and PI filters before insertion or recall.
- **Goal → Plan → Action loop:**
    - **Goal normalization:** convert vague asks into SMART goals + constraints.
    - **Planner:** choose among heuristic task graphs, MCTS/UCT for branching spaces, or linear-temporal plans with preconditions/effects.

    - **Progress guards:** define “done,” “stuck,” and “unsafe” predicates; early abort on violating constraints.

- **Verifiers (make steps checkable):**
    - **Syntactic:** JSON schema, type checks, API contracts.
    - **Semantic:** unit and property-based tests, invariants (idempotency, monotonicity), constraint solvers for feasibility.
    - **Cross-checkers:** redundancy (two tools, two prompts, or two models) with adjudication.
    - **Human-in-the-loop gates:** require approval above risk/impact thresholds.
- **Execution sandboxes:**
    - **Isolation:** per-tool containers/VMs; read-only by default; strict network egress allowlists.
    - **Resource budgets:** CPU/GPU/time/IO quotas; syscall/FS monitors; deterministic timeouts.
    - **Secrets handling:** short-lived tokens via broker; never echo secrets; least privilege by scope and duration.
    - **Forensics:** tamper-evident logs (hash chain), full input/output capture, replay seeds.

Checklist: each step must be *plannable*, *verifiable*, and *reversible*. No tool call without (goal, preconditions, budget, expected outputs, fallback).

5.2 SLAs for tasks: cost, time, safety, and receipts

- **Task SLA = (objective, constraints, acceptance):**
    - **Objective:** measurable target (accuracy≥x, coverage≥y, recall≥z).
    - **Constraints:** max cost $C, max wall-time T, safety class S, privacy level P, jurisdiction J.
    - **Acceptance tests:** deterministic checks + stochastic spot checks; golden cases + canaries.

- **Budgets and metering:**
    - **Cost:** dollars, tokens, API credits, energy (J), human minutes.
    - **Time:** hard deadline vs soft target; slack scheduling; preemption rules.
    - **Risk:** classify tools and actions (R1–R4); cap cumulative risk per job; raise HITL above threshold.
- **Receipts & provenance (proof you did what you claim):**
    - **Action receipts:** {tool, version, inputs hash, outputs hash, start/end time, resource burn}.
    - **Data lineage:** source URIs, content hashes, license/consent tags, transformations.
    - **Attestation:** signature from sandbox + verifier; optional remote attestation (TEE) for high-assurance runs.
    - **SLO accounting:** rolling p50/p95 latency, success rate, false positive/negative, rework rate.
- **Degradation & escalation:**
    - **Graceful degrade:** swap to cheaper tool/model; reduce batch size; pause noncritical subgoals.
    - **Escalation ladder:** auto-retry → alternative tool → simplified objective → human review.
    - **Stop conditions:** burn-rate breach, anomaly detection (e.g., repeated near-duplicates), or policy violation.

Checklist: no agent run starts without an SLA; no run ends without receipts. Report "spent vs budget" and "met vs promised."

5.3 Tool ecosystems (code, web, robots): API design for agency

- **Design principles for agent-facing APIs:**
    1. **Declarative over imperative:** describe *what* (query/spec) not *how* (clicks).
    2. **Schemas everywhere:** JSON/OpenAPI for arguments and results; include units and ranges.
    3. **Idempotency:** provide idempotency keys; retries must not duplicate side effects.

4. **Determinism & pagination:** stable ordering, cursors, bounded page sizes.
5. **Permissions by scope:** per-call scopes; fine-grained resource selectors; expirations.
6. **Dry-run mode:** return predicted effects/quotes without committing.
7. **Test doubles:** sandbox simulators with canned traces for offline planning.

- **Code tools (compilers, package managers, CI):**
  - **Inputs:** code blobs + build matrix.
  - **Guards:** SBOM generation, supply-chain pinning, network block during build, unit tests before deploy.
  - **Outputs:** artifacts with checksums, test summary, coverage.
- **Web/data tools (search, crawl, RAG):**
  - **Inputs:** query + purpose + domains/recency bounds; legal/usage constraints.
  - **Guards:** robots/policy compliance, deduping, source diversity quotas.
  - **Outputs:** snippets + citations + license flags; embedding caches with TTL.
- **Ops/Cloud tools (deploy, scale, observe):**
  - **Inputs:** declarative spec (service, version, SLOs).
  - **Guards:** canary %, rollback triggers, error budgets, policy-as-code checks.
  - **Outputs:** deploy receipt, live metrics endpoints, rollback token.
- **Robotics/physical tools:**
  - **Model:** skills library with preconditions/effects; state estimator + safety envelope.
  - **Guards:** geofences, force/velocity limits, human-proximity modes, E-stop channels.
  - **Proof of work:** task-video hash, pose/force traces, anomaly flags.
- **A minimal, agent-ready tool spec (illustrative):**
- {
- "name": "purchase_order.create",

- "purpose": "Commit to buy items",
- "args_schema": {
- "items": [{"sku": "string", "qty": "int>0"}],
- "ship_to": "address_id",
- "max_total_usd": "float>=0",
- "idempotency_key": "string"
- },
- "constraints": {
- "jurisdiction": ["US-CA","US-TX"],
- "supplier_whitelist": ["SUP-123","SUP-456"]
- },
- "effects": ["inventory_reserved","funds_authorized"],
- "modes": ["dry-run","commit"],
- "returns": {"po_id":"string","total_usd":"float","eta_days":"int"},
- "safety": {"risk_class":"R3","requires_human_above_usd":5000}
- }
- **Observability & feedback:**
    - **Tracing:** per-call spans with tool/version; link to SLA and receipt IDs.
    - **Telemetry for learning:** success labels, latency/cost, policy near-miss; feed a bandit to choose among tools/providers.
    - **Drift sentinels:** alert on schema changes, rising failure types, or quality regressions.

Checklist: make tools easy to *ask correctly* (schemas, examples), safe to *use wrongly* (idempotency, dry-run, scopes), and trivial to *audit* (receipts, traces, citations).

Section takeaway: An agent is a planner/executor constrained by budgets and policy. It earns trust by (1) remembering responsibly, (2) proving each step via verifiers and receipts, (3)

operating inside sandboxes with least privilege, and (4) using well-specified tools whose APIs are built for autonomy—declarative, idempotent, testable, and observable.

6. Society: Institutions of Multi-Agent Coordination

6.1 Roles, contracts, auctions, reputation: mechanism design in practice

- **Roles as capability + duty bundles**
    - *Producer* (offers tasks/resources), *Consumer* (requests outcomes), *Broker* (matches & prices), *Verifier* (tests, certifies), *Custodian* (keys, data, rights), *Arbiter* (dispute finalizer).
    - Each role ships with: scopes, spending limits, escalation rules, and revocation paths.
- **Contracts (from intent to enforceable exchange)**
    - *Offer spec:* what, by-when, for-how-much, with-what evidence.
    - *Guarded effects:* preconditions, postconditions, and revert conditions.
    - *Payment rails:* holdbacks, milestones, clawbacks; split settlement on partial success.
    - *Receipts:* content-hash of inputs/outputs, tool versions, compute/energy burn.
- **Auctions & matching (clearing scarce capability)**
    - *Single-shot:* first-price, second-price (Vickrey), uniform-price for batches.
    - *Combinatorial:* bundle bids for interdependent tasks; XOR constraints to prevent double-selling capacity.
    - *Dynamic markets:* continuous double auction; market makers provide quotes; throttles for volatility.
    - *Reserve & floors:* protect against underbidding that jeopardizes SLOs.
- **Reputation & staking (skin in the game)**
    - *Scores:* rolling success rate, p95 latency, policy violations, audit findings.
    - *Decay & context:* recent work weighs more; domain-specific scores avoid cross-task pollution.

- *Stakes/bonds:* slash on provable breach; unlock after challenge window.

- **Mechanism primitives (IC/IR in mind)**
  - *Individual Rationality (IR):* expected utility >= 0 for truthful participants.
  - *Incentive Compatibility (IC):* truthful revelation is a best response.
  - *Budget Balance (BB):* payments in >= payments out (or planned subsidy).
  - *No free lunch:* you can typically satisfy at most two of {IC, efficiency, BB} without assumptions.

Checklist: every market exposes (roles, contract schema, clearing rule, proof/receipt format, reputation policy, staking), all machine-readable.

6.2 Conflict resolution: arbitration, audits, and rollback

- **Failure taxonomy**
  - *Spec mismatch* (bad contract), *Execution defect* (tool/model bug), *Evidence defect* (missing or forged receipts), *Policy breach* (safety/rights).

- **Fast paths before escalation**
  - *Auto-reconcile:* re-run with stricter verifiers or alternate provider inside same budget.
  - *Graceful degrade:* deliver subset with proportional payment.
  - *Swap-in:* replacement agent via standing market order.

- **Arbitration ladder**

1. *Negotiation window:* parties propose make-goods; timer-bound.
2. *Mediator bot:* applies policy/precedent, recommends split settlement.
3. *Arbiter of record:* bound decision; attaches cryptographic ruling and rationale.

- **Audits (make truth reconstructable)**
  - *Trace bundles:* hash chain of actions, signed tool receipts, environment digests.
  - *Forensic replay:* deterministic seeds, pinned datasets, frozen compiler flags.
  - *Selective disclosure:* zero-knowledge or redacted proofs when data are sensitive.

- **Rollback and state repair**
    - *Two-phase effects:* plan → preview → commit; commits are idempotent and labeled.
    - *Compensating actions:* explicit inverse operations for financial or catalog states.
    - *CRDT/OT for shared docs:* converge without central locks; log causal order.
    - *Kill switch & quarantine:* isolate misbehaving agents; revoke tokens; escrow remaining work.
- **Penalties & learning**
    - *Slashing & bans* proportional to damage and intent.
    - *Root-cause notes* feed reputation features and market risk premia.

Checklist: no contract without a dispute policy; no execution without a trace; no trace without replay; no commit without a compensating path.

6.3 Metrics: throughput, allocative efficiency, incentive-compatibility

- **Throughput & flow**
    - *Task throughput:* completed tasks/time unit (stratify by class).
    - *Queue health:* wait time p50/p95, abandonment rate, bullwhip (variance amplification).
    - *Utilization:* provider busy fraction; look for 60–85% sweet spot (avoid congestion collapse).
- **Allocative efficiency (who gets what)**
    - *Social welfare:* maximize sum_i v_i(x_i) subject to budgets/rights; report gap to best-known feasible.
    - *Price of Anarchy (PoA):* welfare(optimal)/welfare(equilibrium); lower is better.
    - *Fairness:* envy-freeness (no one prefers another's bundle), Gini/Atkinson on utility, share-of-wallet caps.
    - *Coverage:* fraction of demand satisfied within SLA bins; tail shortfall analysis.

- **Truthfulness & strategic behavior**
    - *Regret audit:* average utility gain from profitable misreports in counterfactual simulations.
    - *Collusion signals:* correlated bidding, win rotation; run screens and impose random audits.
    - *Shill resistance:* detect self-trading loops via graph analytics on counterparties.
- **Reliability & integrity**
    - *SLO attainment:* p95 latency/accuracy/cost vs promised; error-budget burn rate.
    - *Reputation stability:* drift in scores vs event rate; false-positive/negative audit rates.
    - *Dispute rate:* per 1,000 tasks; mean time to resolution; rollback success rate.
- **Cost, carbon, compliance**
    - *$/task & $/SLO,* including rework.
    - *J/task & kgCO2e/task* (record PUE, energy mix).
    - *Policy adherence:* violation rate per policy; auto-blocked attempts vs allowed.

Minimal scorecard (per epoch):

- throughput, p95 wait, utilization
- welfare achieved / welfare upper bound
- PoA, fairness index, coverage by SLA
- SLO attainment, dispute rate, MTTR
- $/task, J/task, violation rate

Section takeaway: Multi-agent “society” is not a buzzword; it’s a market with contracts, clearing rules, evidence, and courts. Build in roles, receipts, and reversible state so disputes are cheap; choose mechanisms that keep IR/IC close enough while watching throughput and welfare; and publish a scorecard that makes the coordination quality legible.

7. Autonomic Systems: Self-Monitoring, Self-Repair

7.1 Control loops over SLOs (latency, safety, carbon, cost)

- **Make SLOs first-class control objectives**
    - Latency: target p95/p99 for end-to-end and per-stage.
    - Safety: upper bounds on risk scores, violation rate ≈ 0 within a confidence band.
    - Carbon: limit $kgCO_2e$/task via power caps, PUE awareness, grid-mix signals.
    - Cost: $/task ceilings; minimize under quality constraints.
- **MAPE-K loop (Monitor→Analyze→Plan→Execute, over Knowledge)**
    - **Monitor:** high-cardinality telemetry (traces, metrics, logs, events, energy, policy hits).
    - **Analyze:** SLO error = target − measured; detect drift/anomalies; estimate headroom.
    - **Plan:** compute an action set {scale, route, fuse, quantize, shed, reprioritize}.
    - **Execute:** safe actuators with guardrails and rollback tokens.
- **Controllers to use**
    - **P-only / PID:** simple actuators (replica count, concurrency). Anti-windup + rate limits to avoid thrash.
    - **MPC (model predictive control):** multi-SLO trade-offs with forecast constraints (e.g., keep latency ≤ L while minimizing $ and J).
    - **Multi-objective scheduling:** scalarize with weights or treat as constrained optimization (min cost subject to latency ≤ L, risk ≤ R).
- **Actuation surfaces (examples)**
    - Capacity: autoscale (h/v), batch size, max in-flight.
    - Quality: model/dtype/quantization tier, cache ratio, retrieval depth.
    - Routing: topology-aware placement, traffic split, circuit breakers.
    - Energy: DVFS, clock capping, job migration to greener regions.
    - Safety: stricter filters, require HITL, reduce temperature/creativity.

- **Stability hygiene**
    - Sample/hold periods separate from control periods.
    - Deadbands and hysteresis to prevent flip-flop.
    - SLO *error budgets* to absorb burstiness without overreacting.

Checklist: every SLO has a sensor, an actuator, a controller, a test for stability, and a rollback plan.

7.2 Digital twins, causal monitoring, root-cause toolchains

- **Digital twins (fidelity tiers)**
    - **Black-box twins:** learned surrogates from traces; fast what-if testing for scale/latency/cost.
    - **Grey-box twins:** structure from queueing/flow models plus learned residuals (captures hotspots and caches).
    - **White-box twins:** physics/semantics first (control charts for robots, thermal/IR-drop models for hardware), validated by telemetry.
- **Uses**
    - Capacity planning, placement, energy/cost forecasting, safety envelope checks, failure rehearsal ("chaos twins").
- **Causal monitoring**
    - Maintain a causal graph of components/signals (service deps, queues, caches, fabrics, safety filters).
    - **Change-point & anomaly detection:** seasonal baselines, Bayesian online CPD, robust z-scores on residuals.
    - **Counterfactual probes:** do-operator A/Bs on twins: "If I scaled shard-B +20%, would p99 latency drop?"
- **Root-cause analysis (RCA) pipeline**

1. **Symptom clustering:** group alarms by topology and time (reduce alert storms).
2. **Localize:** blame assignment via dependency graph + Granger/PCMCI time-series causes.

3. **Explain:** attach *evidence cards* (before/after plots, diffs in deploy, config, traffic mix).
4. **Propose fix:** minimal-blast radius actions with predicted SLO impact from the twin.
5. **Validate:** shadow or canary in prod; compare observed vs predicted deltas.

- **Observability substrate**
    - **Traces:** end-to-end spans with baggage (model id, dtype, batch, cache-hit).
    - **Metrics:** RED/USE (Rate, Errors, Duration / Utilization, Saturation, Errors) + energy, cost, policy hits.
    - **Logs:** structured, sampled; link to spans.
    - **Provenance:** hash-chained receipts for data, code, and policy versions.

Checklist: no alert without topology context; no fix without a twin-predicted effect; no resolution without an evidence card.

7.3 Fail-operational design: graceful degradation and recovery budgets

- **Design for *continue to operate*, not just fail-safe**
    - **N+1 / N+M redundancy:** replicas, zones, diverse providers; quorum-tolerant consensus.
    - **Degradation ladders:** tiered behaviors when resources shrink:
        - L3: full-fidelity (max quality/features).
        - L2: cheaper model/path (quantized, less retrieval, smaller batch).
        - L1: cached/approximate answers, reduced features.
        - L0: minimal safe service (static responses, outage banner, queue drain).
    - **Feature flags:** instant toggles tied to SLO controllers; pre-baked safe configs.
- **Budgets & contracts**
    - **Error budgets:** allowed SLO violations per window; burn-rate alarms drive change freezes or rollbacks.
    - **Recovery Time Objective (RTO) / Recovery Point Objective (RPO):** time to restore service / allowable data loss; commit compensating actions if RPO breached.

    - **Energy & thermal budgets:** throttle plans when hitting power/temperature caps; prioritize critical loads.

- **Isolation & blast-radius control**
    - Bulkheads (shard by tenant/region), circuit breakers, backpressure with priority queues.
    - Idempotent APIs + saga/compensations for multi-step writes.
    - Watchdogs and “dead-man’s switch” policies for autonomous subsystems.
- **Readiness drills**
    - Chaos experiments (fault injection, packet loss, node kill, clock skew).
    - Game-day playbooks with clear *abort* and *escalate* criteria.
    - Cold-start rehearsals (cache empty, scaler zero) and brownout drills (power-cap imposed).
- **Post-incident learning**
    - Blameless retrospective; causal tree; action items with owners and expiries.
    - Update twins, controllers, and playbooks; add new guardrails/tests.

Checklist: define degradation tiers, pre-approve compensations, test chaos regularly, and carry explicit RTO/RPO and error budgets as configuration—not folklore.

Section takeaway: Autonomic systems turn SLOs into closed-loop control problems, use digital twins and causal tooling to *decide* rather than guess, and stay useful under stress through fail-operational patterns. The payoff is reliability that scales with complexity: measurable, explainable, and continuously improvable.

8. Objective Layer: Proofs, Rights, and Accountability

8.1 Proof-carrying code, attestations, verifiable logs, watermarking

- **Proof-carrying code (PCC)**
    - *Idea:* ship programs with a machine-checkable proof that key properties hold (e.g., memory safety, no network egress beyond allowlist, bounded cost).

    - *Workflow:* producer emits {binary, spec, proof}; consumer runs a small checker before execution. Proofs can be classical SMT/ATP certificates or zero-knowledge for sensitive properties.
    - *Targets to prove:* safety invariants, resource bounds (time/space/J), data-usage constraints, absence of specific side effects, compliance with API contracts.
- **Attestations (saying who/what ran)**
    - *Build attestation:* SBOM, compiler flags, dependency hashes, reproducible build digest.
    - *Runtime attestation:* TEE quote (e.g., measurement of enclave), container image digest, policy version, input/output content hashes.
    - *Remote verification:* relying party checks signatures against a trust root; optional transparency log inclusion.
- **Verifiable logs (making history durable)**
    - *Structure:* append-only Merkle trees with inclusion proofs and periodic checkpoints; cross-log witnessing to resist equivocation.
    - *Content:* action receipts (tool, version, args hash, outputs hash, start/end, cost, energy), policy decisions, audit events.
    - *APIs:* get_inclusion_proof(entry_id), verify_checkpoint(root, signature), range_proof(start,end).
- **Watermarking & provenance for data/models/outputs**
    - *Inputs:* robust media watermarks, dataset lineage tags, license/consent metadata.
    - *Models:* training-time or post-hoc watermarks; copy detection via trigger sets or statistical fingerprints.
    - *Outputs:* invisible text/media watermarks with public verifiers; provenance envelopes that bind source hashes → output hash.

Checklist: no artifact without {SBOM, build attestation}; no execution without {policy spec, proof or policy justification}; no result without {receipt in a transparency log}.

8.2 Privacy and custody: MPC, enclaves, differential accounting

- **Privacy computation menu**
    - **MPC (multi-party computation):** compute f(x1,...,xn) without revealing xi; good for joint analytics and settlement. Choose between garbled circuits, secret sharing, or hybrid.
    - **HE (homomorphic encryption):** limited to small circuits or specialized ops where latency tolerates overhead; often paired with batching.
    - **TEE (enclaves):** run plaintext inside hardware-isolated memory; combine with remote attestation and encrypted I/O.
    - **Hybrid pipelines:** TEE for heavy compute + MPC for cross-party joins; encrypt at rest; minimize cleartext footprint windows.
- **Custody & access control**
    - *Data contracts:* schema + permitted purposes + retention TTL + locality/jurisdiction.
    - *Scopes & leases:* short-lived tokens, least privilege, renewals by policy bot.
    - *Redaction & minimization:* collect only needed fields; deterministic tokenization/pseudonymization with vault-held keys.
- **Differential privacy (DP) & accounting**
    - *Mechanism:* add calibrated noise; track privacy loss with epsilon, delta per query.
    - *Budgeting:* per user/entity DP ledger; deny or coarsen queries that would overspend the budget.
    - *Aggregate reporting:* thresholds, partition selection, contribution bounding to avoid singling out.
- **Lineage & legal posture**
    - *Provenance graph:* link inputs → transforms → outputs; store consent and license edges.
    - *Jurisdictional guards:* geofenced compute, data residency, deletion proofs.
    - *Breach response:* revocation lists, key rotation, and audit-log freeze on incident.

Checklist: every sensitive job declares {purpose, legal basis, DP budget, custody plan}; every cross-party job chooses {MPC/TEE/HE} with a rationale; every dataset has {lineage, consent, TTL, jurisdiction}.

8.3 Governance APIs: machine-readable policy and automatic compliance

- **Policy-as-code (declarative, testable)**
  - *Schema:* rules over subjects, actions, resources, context (time, geo, risk, SLA).
  - *Engines:* OPA/Rego-style or Datalog; sidecar or gateway enforcement; pre-commit checks for code/config.
  - *Versioning:* signed policy bundles with changelogs; staged rollouts and canary policies.
- **Pre-flight & continuous compliance**
  - *Pre-flight:* plan validation (does this deploy/query comply?), impact simulation, exemption requests with expiry.
  - *Continuous:* real-time decisions on each call; policy hits recorded as structured events; automatic quarantine on repeated near-misses.
- **Controls & guardrails surfaced as APIs**
  - *Quota & budget controls:* $/task, J/task, data reads per window; returned in responses to guide callers.
  - *Safety switches:* require_HITL, blocklist/allowlist, temperature/top-k caps by risk tier.
  - *Data governance:* allowed_fields, redaction maps, retention timers; auto-deletion callbacks.
  - *Deployment governance:* canary %, rollback token, error-budget guard.
  - *Evidence on demand:* GET /receipts/{id}, GET /attestations/{run}, GET /policy_decision/{call}.
- **Assurance levels (tiered)**
  - L1: log-only; periodic audits.
  - L2: mandatory receipts + sampling audits; DP budgeting.

    - L3: proofs required (PCC/TEE quotes); pre-commit formal checks; external witness logs.
    - L4: continuous proofs (runtime monitors), dual control for high-risk operations, external regulator feeds.
- **Human governance loop**
    - *Dashboards:* SLOs for compliance (violation rate, mean time to remediate).
    - *Exception workflow:* time-boxed, reasoned, logged; auto-revert.
    - *Policy lint & tests:* unit/property tests; regression suites against incident postmortems.

Checklist: no deploy without policy check; no high-risk action without tier-appropriate assurance; no exception without expiry, owner, and audit trail.

Section takeaway: The objective layer makes *claims* about behavior verifiable. Programs carry proofs, runs carry attestations, histories live in verifiable logs, and privacy/custody are enforced by MPC/TEE/DP rather than promises. Governance becomes an API: machine-readable rules that gate actions, meter budgets, and surface evidence on demand.

9. Co-Designed Matter: From Kernels to Fabrication Recipes

9.1 Inverse design across CMOS, photonics, MEMS, RF, packaging

- **Design–Technology Co-Optimization (DTCO) → System-Technology Co-Optimization (STCO):** move from "pick a process, then design" to "co-solve device, circuit, package, and workload." Treat masks and materials as compiler targets.
- **Inverse design loop (generic):**
    1. *Spec:* target ops (e.g., GEMM/attention), bandwidth, latency, jitter, thermals, carbon.
    2. *Parametric space:* device (fin/nanosheet widths, threshold sets), interconnect (stack, pitch), photonic cells (MZI/microring), MEMS geometries, RF stackups, package traces/vias.
    3. *Differentiable/adjoint simulators:* EM/RC/thermal/optical/mechanical solvers produce gradients; surrogate models cover gaps.

4. *Optimizers:* multi-objective (perf/W, area, yield, carbon), with manufacturability constraints (min feature, OPC/ILT limits, density windows).
5. *Verification:* corner/Monte Carlo, variability (RDF, LER), aging (BTI/HCI/EM).
6. *Recipe emit:* masks, OPC/ILT patterns, deposition/etch sequences, anneal profiles, bonding temps.

- **CMOS focus:**
    - *Cell libraries by kernel:* attention-centric libs (wide SRAM ports, high-fan-out buffers), GEMM-heavy libs (taller metal for current, dense local interconnect).
    - *Memory-first macros:* multi-bank SRAM with near-compute datapaths; bit-cell options (6T/8T) tuned for voltage corners.
    - *Power delivery co-design:* backside PDN, on-die regulators, IR-aware placement.
- **Silicon photonics:**
    - *Use cases:* chip-to-chip/inter-rack fabrics; in-package optical I/O to escape copper walls.
    - *Cells:* MZI meshes (broadband, larger), microrings (compact, need tuning), grating couplers (loss vs pitch), germanium photodiodes, III-V/Si lasers (hybrid).
    - *Inverse optics:* place/size rings, heaters, and waveguide bends for target λ budgets; add control loops for thermal drift.
    - *Co-packaged optics (CPO):* floorplans that minimize electrical reach from MAC arrays to photonic drivers/receivers.
- **MEMS & micro-actuation:**
    - *Skews toward agents/embodiment:* micro-mirrors, pressure/flow/IMU arrays, micro-pumps.
    - *Co-design:* fuse sensor placement with estimator bandwidth; design Q-factor and damping for control latency targets.
- **RF/mmWave & antenna-in-package:**
    - *Phased arrays:* inverse place/route for beam patterns; thermal + EM coupling constraints.
    - *AiP:* laminate/organic substrate routes as part of the solver (impedance control, via stubs).

- **Advanced litho & masks:**
    - *OPC/ILT as compilation passes:* emit mask shapes that print desired on-wafer contours; penalize hotspots; respect shot count and write time.
- **Packaging as part of the graph:**
    - *2.5D/3D:* interposers, hybrid bonding (face-to-face), TSVs; model warpage and thermal interfaces.
    - *Fan-out & RDL compilers:* auto-route high-BW buses; length-match and skew budgets become constraints.

Checklist: choose simulators that are gradient-friendly, encode manufacturability as hard constraints, co-optimize device–circuit–package, and emit mask + process steps as first-class "artifacts."

9.2 Chiplets and memory fabrics co-evolved with model workloads

- **Why chiplets:** break reticle limits, boost yield, mix process nodes (logic on N, SRAM/analog on N+1), and iterate subsystems independently.
- **Interconnect choices:** UCIe die-to-die, proprietary mesh fabrics, BoW; treat lane count, speed, and equalization as tunables in the co-design.
- **Memory is the new core:**
    - *HBM stacks & beyond:* size channel count vs model's activation/KV footprints; select burst length and prefetch to match attention/MLP rhythm.
    - *CXL/pooled memory:* for inference clusters, let multiple accelerators mount a shared KV pool; optimize path length vs QoS.
    - *Near-/in-memory compute:* SRAM/embedded-DRAM MAC tiles for low-precision ops; schedule to minimize read-write energy.
- **Topology shaped by kernels:**
    - *Attention-centric:* star or dual-rail fabrics for all-to-all; KV-cache sharding across chiplets; lightweight multicast for K broadcast.
    - *GEMM-centric:* 2D torus/mesh; local scratchpads sized to tile shapes; multi-rank HBM skewed toward MLP layers.

- *MoE workloads:* all-to-all heavy—cluster experts per switch domain; bake placement into the compiler.

- **Heterogeneity on purpose:**
  - *Logic chiplet:* tensor/attention engines + schedulers.
  - *Memory chiplet(s):* HBM controllers, KV compressors, prefetchers.
  - *I/O/optics chiplet:* SerDes/laser drivers, retimers.
  - *Security/service chiplet:* roots of trust, metering, attestation engines.
- **Software contracts:** expose NUMA-like hints up the stack (bandwidth classes, preferred placement). Compilers schedule graph shards to chiplets with cost models for hop count and contention.

Checklist: start from model traces (bytes/op over time), derive fabric and chiplet budgets, and lock software/runtime contracts before physical partitioning.

9.3 Closing the loop: cost models, yield, and field telemetry

- **Transparent cost model (PPA+C):**
  - *Die cost:* wafer_cost × (dies/wafer × yield)^−1; yield via Poisson/Murphy on defect density and critical area.
  - *NRE:* masks, IP, EDA, bring-up; amortize by volume and time-to-breakeven.
  - *Package & test:* known-good-die probing, burn-in, test seconds (ATE $/s), assembly yields.
  - *Power & carbon:* watts at workload mix, cooling penalty (PUE), region grid mix → $kgCO_2e$/unit and per task.
  - *Service cost:* RMA rate, field failure (FIT), spares, firmware maintenance.
- **Why chiplets help yield:** smaller dies ⇒ lower defect exposure; bin parts by speed/leakage; compose SKUs (good logic + slower memory) rather than scrap.
- **Reliability & aging budgets:**
  - *On-die sensors:* ring-osc arrays (process/aging monitors), thermal diodes, droop detectors, EM sentinels, error counters (ECC, parity).

    - *RAS features:* retry, sparing, ECC scrubbing, lane de-rate; fuse-controlled A/B logic for field experiments.
    - *Design for derate:* ship at V/f that leaves lifetime margin; controllers adapt with telemetry.
- **Field telemetry → next revision:**
    - *Silicon Lifecycle Management (SLM):* collect per-part telemetry (with privacy), correlate failures with layout/process features; feed back into placement rules and library sizing.
    - *Twin reconciliation:* align measured perf/thermals/jitter with pre-silicon models; update surrogates and guard-bands.
    - *A/B at scale:* controlled rollouts of firmware/voltage tables; compare SLOs, error budgets, and $/task.
- **Yield learning & DFM updates:**
    - *Hotspot mining:* pattern matching on failing locations; ban motifs in PDK rules.
    - *Parametric yield:* widen corners that bite (e.g., sense-amp margins), relax density only where yield justifies area hit.
    - *Mask respins:* prioritize ILT fixes with biggest Pareto lift (yield × volume × margin).
- **Business loop:** sync BOM + cost deltas with product pricing and cloud tariffs; tie SKU mix to real workload demand (e.g., attention-heavy vs GEMM-heavy customers).

Checklist: publish a living PPA+C (cost & carbon) model, stream SLM telemetry into twin + library updates, and gate new tape-outs on demonstrable yield/MTBF improvements and $/SLO gains.

Section takeaway: “Co-designed matter” treats hardware, packaging, and even masks as compiler targets driven by the workload’s math. Use inverse design to search device–circuit–package spaces, assemble systems from chiplets and memory fabrics shaped by real model traces, and close the loop with cost/yield telemetry so each tape-out is measurably better in performance, watts, dollars, and reliability.

10. Embodied Mesh: World-Scale, Resilient Compute

10.1 Edge swarms, intermittent power, local learning and bargaining

- **Edge swarm model:** thousands→millions of heterogeneous nodes (phones, cameras, drones, meters, kiosks, micro-robots) cooperating under local constraints (power, bandwidth, privacy, regulation).
- **Energy first:** intermittent power (solar, kinetic, duty-cycled grid) ⇒ *design for brownouts*.
    - Sleep/wake schedules; **intermittent computing** (checkpointed RAM/NVM); task fragments sized to energy packets.
    - Harvest-aware schedulers: prioritize short, high-value jobs when SoC < θ.
- **Local learning:** keep data on device; ship *updates, not raw logs*.
    - **Federated/stream learning:** FedAvg/FedProx/FedNova with client selection by freshness/trust; on-device quantized gradients; secure aggregation.
    - **Tiny adapters:** LoRA/adapter layers for domain drift; periodic, budgeted distillation into a small local model.
- **Neighborhood bargaining:** nodes trade work and resources.
    - **Micro-markets:** tokens/credits for relays, labeling, sensor time.
    - **Price signals:** higher price during energy/coverage scarcity; rebates for redundancy.
    - **Fairness knobs:** per-tenant quotas, anti-hoarding rules, service class reservations.
- **Work decomposition:** declarative tasks → tiles with **SLO slices** (latency budget, safety tier, privacy tier, energy cap).
    - Opportunistic placement: prefer nodes with (co-located data ∧ green energy ∧ good RF ∧ proper trust level).
    - Gossip discovery with TTL to avoid flooding.

Checklist: energy-aware runtime, local training with secure aggregation, micro-markets for relays, and task tiling that carries per-tile SLO/ethics labels.

10.2 Topologies for robustness: store-and-forward, DTN, CRDTs

- **Mixed connectivity is the norm:** some links high-BW/low-latency, many links lossy or absent. Design for *eventual* not continuous connectivity.
- **Store-and-forward/DTN (Delay/Disruption-Tolerant Networking):**
    - **Bundle semantics:** messages carry custody transfer, expiries, and multiple next-hop options.
    - **Opportunistic links:** buses, drones, passing phones act as ferries.
    - **Routing:** PRoPHET/MaxProp/Spray-and-Wait; replicate under scarcity, converge to single path as stability rises.
    - **Priority lanes:** life-safety and control traffic preempt telemetry/bulk.
- **Overlays and meshes:**
    - **Local meshes:** 802.11s/Thread/LoRa clusters; gateways bridge to fiber/cellular/sat.
    - **Islanded operation:** regions run autonomously (local ledgers, caches, controllers) with *merkleized* state to reconcile on rejoin.
- **Conflict-free replicated data types (CRDTs):** converge state without central locks.
    - **Types:** G-Counter/PN-Counter (usage), OR-Set (registries), LWW-Register/Map (configs), delta-CRDTs for bandwidth thrift.
    - **Use:** job queues, reputations, inventories, soft reservations; **causal metadata** (vector clocks) to explain merges.
- **Resilient caching and naming:**
    - Content-addressable storage; name by hash; any node can serve if it *proves* the chunk.
    - **Witness sets:** small quorum signs “latest known” roots to prevent long-range equivocation.
- **Security in motion (zero trust):** mutual auth per hop; short-lived keys; rotate identities; rate-limit and quarantine suspicious peers; privacy budgets enforced at the edge.

Checklist: DTN bundles with custody and expiry, CRDT-backed shared state, islanding/reconciliation plans, content-addressed caches, and zero-trust sessioning.

10.3 Safety cases and ethics in the loop: what "reliable control" means in the wild

- **Reliability ≠ uptime only; it's controlled obligation under uncertainty.**
    - **Control guarantees:** bounded tracking error, stability margins (gain/phase), passivity where possible; explicit *safe sets* with control barrier functions (CBFs).
    - **Hierarchical loops:** fast reflex layer (safety shield), nominal controller (MPC/PID), and slow planner (agent/society) with veto rights.
- **Runtime safety monitors ("shields"):**
    - Check action proposals against invariants (speed/force/geofence/thermal/current).
    - Enforce *assume-guarantee* contracts between modules; drop to safe mode on violation.
    - **Fail-operational:** degrade gracefully (reduced speed/features) rather than hard stop, unless human life/critical assets at risk.
- **Safety case artifacts (before and during deployment):**
    - **Hazard analysis:** STPA/FMEA; list losses, hazards, constraints, controllers, unsafe control actions.
    - **Assurance evidence:** simulations, adversarial tests, coverage on corner cases, proofs for local invariants, plus **receipts** from on-device monitors.
    - **Operational envelopes:** where the system is allowed to act (weather, crowd density, RF health). Gate entry with sensors and third-party attestations.
- **Ethics and rights as runtime policy:**
    - **Consent & locality:** data never leaves jurisdiction without triggers; per-individual consent tokens; right-to-be-forgotten enforced via key erasure + CRDT tombstones.
    - **Capability caps:** risk-tiered abilities (e.g., no physical manipulation above R2 without human co-presence).
    - **Equity:** service rationing rules during scarcity (medical, emergency comms, then commercial).
    - **Transparency:** on-device *why card* (last k decisions with features used), accessible to auditors and affected parties.

- **Testing the wild, not the lab:**
    - **Field trials with guardrails:** shadow mode → supervised mode → capped autonomy; staged geographic rollout.
    - **Chaos & ethics drills:** inject RF loss, sensor spoofing, crowd anomalies; include *ethical canaries* (ambiguous edge cases) and verify de-escalation behaviors.
    - **Post-incident doctrine:** blameless RCA; publish safety deltas; update envelopes and shields; prove the fix with targeted replays.
- **KPIs that matter:**
    - **Safety:** near-miss rate, intervention rate, time-to-safe, violation per operating hour.
    - **Control:** closed-loop latency, stability margins, actuator duty, thermal headroom.
    - **Societal:** opt-out rate, fairness indices under rationing, complaint resolution time.
    - **Sustainability:** J/task, % green-powered tasks, carbon per delivered outcome.

Checklist: explicit safety envelopes, layered control with runtime shields, machine-readable ethics/policy, audited field trials, and KPIs that include people and planet—not just throughput.

Section takeaway: An embodied mesh treats the world as the computer. It tolerates power loss and broken links, learns where the data live, bargains for scarce resources, reconciles state without central locks, and keeps humans safe by constraining autonomy with real-time ethics and control theory. The result is resilience by design: services that continue—perhaps with fewer features—but do not fail catastrophically when the world behaves like the world.

11. Humanity at Each Rung — Ten Summaries

11.1 Transistor → Reliable Bits

The transistor shrank the cost of certainty. When switches became tiny, cheap, and dependable, knowledge could be copied and computed at scale. Humanity gained radios, calculators, and eventually the fabric of modern communication. The social effect was democratized access to information—and a new dependency on invisible infrastructures whose failures (power, supply chains) can ripple widely.

11.2 CPU → General-Purpose Control

CPUs turned reliable bits into reliable instructions, standardizing how we tell machines what to do. Software ate clerical labor, logistics, and administration, amplifying individual productivity while centralizing power in those who control code and standards. The upside: broad prosperity and convenience. The risk: monocultures and the fragility of systems no single person fully understands.

11.3 GPU → Throughput for Parallel Tensors

GPUs made heavy math cheap. That unlocked real-time graphics, scientific simulation, and the modern AI wave. The cultural effect is immersion (games, AR/VR) and acceleration of discovery (climate, biology), but also an energy footprint that ties cognition to kilowatts and concentrates capability where capital can afford the fabs and clusters.

11.4 Model → Learned Capability

Differentiable programs shifted us from programming features to training behaviors. This widened participation—non-coders can instruct systems via data and prompts—and raised hard questions about bias, provenance, and accountability. Models amplify what we measure; they also mirror what we ignore. Society gets new tools for language, vision, medicine—and a need for new norms of evidence and consent.

11.5 Agent → Goal-Directed Autonomy

Agents take goals, keep memory, use tools, and return receipts. They move work from “I’ll do it later” to “it’s already done.” For people, this is time returned and cognitive load reduced; for firms, it’s process elasticity. The new hazards are silent errors at machine speed, subtle policy breaches, and displacement without adequate reskilling—mitigated only by budgets, proofs, and human-in-the-loop gates.

11.6 Society → Multi-Agent Institutions

Markets of agents—roles, contracts, auctions, reputation—scale coordination beyond any team. We gain faster matching of needs to skills, continuous procurement, and transparent service guarantees. We also inherit market failures (collusion, externalities) unless we embed mechanism design, auditing, and fair access. Done well, coordination costs fall; done poorly, inequality hardens behind APIs.

11.7 Autonomic Systems → Self-Monitoring, Self-Repair

Turning SLOs into control loops reduces outages and toil. Systems that watch, plan, and fix themselves raise baseline reliability for medicine, mobility, finance, and communication. The

human effect is fewer crises and more predictable services—paired with a shift in labor from firefighting to designing twins, controllers, and playbooks that keep complexity tame.

11.8 Objective Layer → Proofs, Rights, Accountability

When programs carry proofs and runs carry attestations, trust scales beyond reputation to evidence. People gain enforceable rights over data use, regulators gain continuous visibility, and operators gain defensible compliance. Friction rises in the short term (proofs aren't free), but the payoff is resilience against fraud, abuse, and denial—computing that can be believed, not just observed.

11.9 Co-Designed Matter → Idea-to-Artifact Loops

Inverse design and chiplet fabrics let workloads shape devices and packages directly. Hardware evolves at the tempo of software releases; niche communities can mint specialized matter. This democratizes invention while exposing society to faster hardware churn, e-waste risks, and geo-economic chokepoints. Cost/yield telemetry and carbon accounting become civic, not just technical, duties.

11.10 Embodied Mesh → World-Scale, Resilient Compute

Compute spreads into streets, fields, homes, and bodies—learning locally, bargaining for scarce energy, and surviving disconnection. Humanity gains services that persist through storms and outages and that adapt to local needs. The ethical bill comes due: safety cases, consent, and fairness must run at the edge, or autonomy will fail the very communities it intends to serve.

Section takeaway: Each rung traded detail for capability and pushed new obligations upward—evidence, control, and care. The ladder's promise is abundance with accountability; its failure mode is power without proofs.

12. Man–Machine Interaction in the Embodied Mesh

12.1 Co-agency, not "user vs system"

- **Shared locus of control:** people set goals and boundaries; local nodes plan and act under SLOs; both sides keep receipts.
- **Roles in pairs:** human roles (resident, paramedic, farmer, dispatcher, regulator) map to mesh roles (observer, planner, executor, verifier, custodian).
- **Contract of work:** each task carries a small SLA bundle: purpose, time/cost caps, privacy tier, safety tier, success tests, and rollback path.

12.2 Interfaces that fit the moment

- **Low-friction asks:** speech, taps, paper QR, glove buttons; short, domain-legal vocab ("survey-row 17", "escalate-medical", "shed-2kW-now").
- **Return channels:** haptics and lights for reflex cues; on-device "why card" (last k decisions + features used) for post-hoc understanding.
- **Attention design:** agents meter notifications by risk and relevance; batch the rest. Local quiet hours and incident overrides are first-class controls.

12.3 Consent, custody, and local first

- **Consent tokens:** per person/place, scoped ("air quality, 24 h, research use=no"); expire by default.
- **Local data gravity:** learn on device; export updates, not raw streams; redaction by schema, not by hope.
- **Right to be forgotten:** key erasure + CRDT tombstones; receipts show when and where deletion propagated.

12.4 Safety envelopes with human override

- **Guardrails in layers:** fast safety shield (force/geo/temperature limits) > nominal controller (MPC/PID) > planner. Any layer can veto upward plans that violate invariants.
- **Human override:** explicit channels for stop, slow, or hand-drive; dual acknowledgment for re-arm.
- **Graceful degrade:** feature ladders (L3 full → L2 cheaper → L1 cached → L0 minimal safe) chosen by policy and power.

12.5 Trust calibration and learning together

- **Transparent uncertainty:** summaries include confidence, alternatives, and what data were *not* seen.
- **Feedback that teaches:** one-tap labels ("acceptable", "unsafe", "nuisance") retrain local policies; bandits allocate future attention and routes.
- **Skill transfer:** tiny adapters (LoRA) capture local know-how; periodic distillation keeps models small and aligned with people's practice.

12.6 Workflows across power and packets

- **Intermittent power:** tasks chopped into energy-sized fragments; progress survives brownouts; priorities track people and risk, not just throughput.
- **Disrupted links:** DTN bundles with custody and expiry; store-and-forward via buses/drones; islanded operation reconciles later by hash.
- **Micro-markets:** tokens for relays, labels, and spare power; price signals prevent free riders; equity rules protect essential service tiers.

12.7 Accountability you can carry to a meeting

- **Receipts:** {who, what, when, inputs hash, outputs hash, tool versions, cost J/$, policy hits}, signed by the sandbox; printable QR for offline checks.
- **Explainable incidents:** evidence cards tie symptoms to fixes; “show work” is the default, not a favor.
- **Appeals and arbitration:** time-boxed negotiation → mediator bot → arbiter of record; compensations are pre-coded, not improvised.

12.8 Human factors: dignity, effort, and failure costs

- **Dignity by default:** systems ask before seeing; degrade service rather than pry; show people what is stored about them.
- **Cognitive load budgets:** UI and alerting are measured; nuisance alarms count against error budgets.
- **Failure economics:** time-to-safe, rework minutes, and social impact (missed clinic, spoiled crop) are tracked like latency and dollars.

12.9 Field patterns (concrete vignettes)

- **Paramedic + drone:** medic says “scout stairwell A”; drone flies inside safety envelope; returns thermal map, confidence, and route; any human gesture “flat palm” stops motion.
- **Farmer + micro-grid:** phone shows “irrigate row 17, 12 min, 0.8 kWh, water budget ok”; farmer taps “halve water, extend time”; controller replans and logs carbon saved.
- **Market + kiosk:** shopper opts-in for translation; device watermarks output, logs consent, and auto-expires at day’s end.

12.10 Minimal scorecard (people + machines)

- **Safety:** near-miss/hr, intervention rate, time-to-safe.
- **Service:** task success %, p95 completion time under brownout/DTN.
- **Burden:** alerts/person/day, average handling time, opt-out rate.
- **Fairness:** service coverage across neighborhoods; rejection/latency gaps.
- **Stewardship:** J/task, % green power, kgCO2e/task, e-waste return rate.
- **Trust:** complaint resolution time, audit pass rate, deletion confirmation time.

Section takeaway: In the embodied mesh, humans and machines are co-workers under contract: people set aims and limits; devices act locally, explain themselves, and prove what they did; both share power budgets, data ethics, and blame-free learning after faults. The interaction is successful when everyday users can *ask simply, override safely, verify easily,* and *benefit locally*—even when the grid flickers and the network frays.

Epilogue: Whose Vision Is This?

It is tempting to say this ladder belongs to engineers—that the transistor is theirs, the CPU theirs, the GPU theirs, the model theirs, and the rest a procession of technical inevitabilities. But the rungs exist because people kept asking larger questions than any single device could hold. The ladder is communal: physicists who tamed electrons; mathematicians who made logic bear weight; machinists who kept tolerances; teachers who turned abstractions into habits; caregivers who asked for reliability over spectacle; regulators who insisted on rights; farmers who needed weather that lies less; children who wanted stories in their own language. The vision is not authored by a profession. It is authored by need.

Still, a ladder is also an argument. Ours argues that complexity must purchase accountability—that every new competence must carry a receipt. It argues that scale without safety is vandalism, and safety without agency is paternalism. It argues that proofs are not shackles but circulation, the hemoglobin of trust. If that sounds moral as much as technical, it is because the most technical thing we now do is to bind power to measure and action to answer.

Is this the machine's vision, then? Machines do not hold visions; they hold objectives. Left alone, they optimize where the gradients slope. Vision comes from us: from what we count and what we refuse to count, from which constraints we elevate to laws and which we leave as defaults, from what we are willing to stop doing when a metric starts to lie. In the embodied

mesh, our preferences become policy, and our policies become physics. If the world begins to feel computational, it is because we have let our values be compiled.

But the paper has insisted on reciprocity. The “objective layer” exists so that people can ask, “Show me.” The “autonomic” exists so they can ask, “Fix it.” The “society” exists so they can ask, “Who is responsible?” The “agent” exists so they can ask, “Can you handle this for me—within these limits?” The “model” exists so they can ask, “Can you learn this pattern without stealing its soul?” The “GPU/CPU/transistor” exist so those answers arrive before relevance expires. None of these are merely technical accommodations; they are constitutional clauses of a new civic instrument.

Whose vision is this? It belongs to the person who says “stop” and means it, and to the system that hears “stop” as a first-class instruction. It belongs to the clinic that runs during storms because power was treated as a budget, not a wish. It belongs to the teacher in a quiet town whose students can debug a policy because the policy is code, not rumor. It belongs to the operator whose pager goes off less because twins and controllers carry the night shift. It belongs to communities that receive the benefits of autonomy without surrendering their right to consent, to opt out, to demand deletion, to ask why.

There is a humbler answer, too. The ladder is a sketch over moving water. Technology drifts; goals recede; the best ideas arrive from the margins. Tomorrow will redraw sections we thought definitive. That is not a defect but a discipline: to build so that revision is survivable, to measure so that regret is containable, to design so that failure degrades gracefully rather than catastrophically.

So: the vision is ours only while we are willing to keep proving it. Not with slogans, but with receipts. Not with myth, but with mechanisms that ordinary people can interrogate. If, years from now, someone asks whether this future was inevitable, let the answer be no. Let it be chosen. Let it be the kind of choice that leaves the world measurably safer, fairer, and more intelligible—because the rungs we climbed were strong enough to bear both power and responsibility, and because we never let competence outrun care.

Transistor / CMOS → Reliable Bits

- **People:** Gordon Moore, Robert Noyce, Jack Kilby, Carver Mead, Lynn Conway, Tsugio Makimoto, Mark Horowitz.
- **Orgs:** Bell Labs; **Intel**, **TSMC**, **Samsung**, **GlobalFoundries**; **IMEC**, **CEA-Leti**; SkyWater + open PDK collaborators.

CPU → General-Purpose Control

- **People:** John Hennessy, David Patterson, Sophie Wilson, Steve Furber, Krste Asanović, Margaret Martonosi.
- **Orgs: ARM**, **RISC-V International**, **IBM**, **AMD**, **Apple**; UC Berkeley RISC-V/ASPIRE; **OpenHW Group**.

GPU / Throughput Compute

- **People:** Jensen Huang, Lisa Su (GPU heritage), Bill Dally.
- **Orgs: NVIDIA**, **AMD**, **Intel** (GPU), **MLCommons** (benchmarks), **Khronos** (CUDA alternatives, SYCL/OpenCL lineage).

Model / Differentiable Programs

- **People:** Geoffrey Hinton, Yann LeCun, Yoshua Bengio; Demis Hassabis, Oriol Vinyals; Andrej Karpathy; Fei-Fei Li.
- **Orgs: DeepMind**, **OpenAI**, **Anthropic**, **Meta FAIR**, **Google DeepMind/Brain lineage**, **Microsoft Research**, **Hugging Face**, **Mistral**, **EleutherAI**, **LAION**, **Allen Institute for AI**.

Agent / Goal-Directed Autonomy

- **People:** Stuart Russell, Leslie Kaelbling & Tomás Lozano-Pérez, Sergey Levine, Pieter Abbeel, Chelsea Finn.
- **Orgs: CMU RI**, **MIT CSAIL**, **Berkeley AI Research**, **Toyota Research Institute**, **Boston Dynamics AI Institute**, **NNAISENSE**; tool-ecosystem stewards like **LangChain**, **LlamaIndex**, **OpenRAG**.

Society / Mechanism Design & Markets

- **People:** Alvin Roth, Paul Milgrom, Preston McAfee, Noam Nisan, Tim Roughgarden.
- **Orgs: Mechanism Design for Social Good (MD4SG)**, **Stanford MS&E/CS** game-theory groups, **OECD** Digital Policy, **Partnership on AI** (AI & labor/market impacts).

Autonomic Systems / SRE & Self-Repair

- **People:** Betsy Beyer, Niall Richard Murphy (SRE), Brendan Burns (Kubernetes), John Wilkes.
- **Orgs: Google SRE**, **Microsoft Azure**, **AWS** (Fault-Isolation, Well-Architected), **CNCF** (K8s, Prometheus, OpenTelemetry), **Netflix** Chaos Engineering.

Objective Layer / Proofs, Rights, Accountability

- **People:** Leslie Lamport (TLA+), Nancy Leveson (STPA), John Rushby (formal methods), Xavier Leroy (CompCert), Gerwin Klein (seL4), Martin Abadi.
- **Orgs & specs: NIST** (AI Risk, Zero Trust), **ISO/IEC JTC 1** AI & security, **IETF** (transparency, logs), **C2PA/Content Authenticity Initiative**, **Sigstore**, **OpenSSF/SLSA**, **seL4 Foundation**, **Galois**, **Trail of Bits**, **OpenDP** (Harvard/MIT).

Co-Designed Matter / Inverse Design, Chiplets, Photonics

- **People:** Mark Papermaster, Bill Dally, Subhasish Mitra, Azita Emami; in photonics: Dirk Englund, Jelena Notaros; Light-at-compute: Nicholas Harris.
- **Orgs: ASML** (EUV/High-NA), **Cerebras**, **Graphcore**, **Lightmatter**, **Lightelligence**, **Ayar Labs**; **DARPA ERI**, **CHIPS Act** programs; **UCIe** consortium; **OpenROAD**/**OpenLane**.

Embodied Mesh / Edge, DTN, CRDTs, Safety

- **People:** Vint Cerf & Kevin Fall (DTN), Martin Kleppmann (CRDTs), Aaron Ames (control barrier functions), Daniela Rus (field robotics).
- **Orgs: LoRa Alliance**, **Thread Group**, **IETF DTN WG**; **Automerge**/**Ink & Switch** (CRDTs); **OpenStreetMap** (citizen data), **Wikimedia**; **ISO 26262** / **UL** / **IEC** safety bodies; **FAA/EASA** (UAS), **NERC** (grid).

Cross-Cutting Stewards (ethics, governance, rights)

- **Civil society & policy: EFF**, **ACLU**, **Access Now**, **Future of Privacy Forum**, **Ada Lovelace Institute**, **OECD**, **UNESCO**, **IEEE** (Ethically Aligned Design), **EU AI Office/EDPB/CNIL/ICO**.
- **Safety & alignment: Center for AI Safety (CAIS)**, **Alignment Research Center (ARC)**, **GovAI**, **Anthropic's RL/constitutional efforts**, **OpenAI Preparedness**, **DeepMind safety**.
- **Standards & measurement: NIST ML/AI** evaluations, **MLCommons** benchmarks, **TLA+**, **Coq/Lean** communities, **SPDX** (software bills of materials).

Communities that "quietly carry" the vision

- **Ops & reliability guilds:** SRE, chaos engineering, incident.io circles.
- **Open-source maintainers:** Linux, Kubernetes, PyTorch/JAX, Triton/TVM, Hugging Face Hub, OpenTelemetry.

- **Citizen networks:** ham radio clubs (DTN relays), community micro-grids, makerspaces with PCB/fab labs.
- **Educators:** curriculum writers bringing verification, ethics, and energy budgets into CS/EE 101.

This vision is midwifed by device physicists and verification mathematicians; by compiler writers and standards lawyers; by reliability engineers who sleep with pagers and organizers who write the consent forms; by teachers who make abstractions survivable and regulators who make power answerable. Any list is incomplete; the measure of our seriousness is whether the receipts—proofs, rights, and repairs—reach ordinary people where they live.

References

1. Transistor, CMOS, and Digital Discipline

- Shockley, W. (1949). The theory of p–n junctions in semiconductors. *Bell System Technical Journal*.
- Bardeen, J., & Brattain, W. (1948). The transistor, a semi-conductor triode. *Phys. Rev.*
- Dennard, R. H., et al. (1974). Design of ion-implanted MOSFETs with very small physical dimensions. *IEEE JSSC*.
- Mead, C., & Conway, L. (1980). *Introduction to VLSI Systems*. Addison-Wesley.
- Ho, R., Mai, K., & Horowitz, M. (2001). The future of wires. *Proc. IEEE*.
- Kahng, A. B. (2018). Scaling: *the* Moore's Law perspective. *SLIP/ISPD Tutorials*.

2. CPU Architecture, Memory, and Virtualization

- Hennessy, J., & Patterson, D. (2017). *Computer Architecture: A Quantitative Approach* (6e).
- Lamport, L. (1979). How to make a multiprocessor computer that correctly executes multiprocess programs. *IEEE TSE*.
- Rosenblum, M. (1995). The design and implementation of a virtual machine monitor. *ACM OSDI*.
- Martonosi, M., et al. (2019). *Computer Architecture Today: Trends and Challenges*. Memos/ACM.

3. GPUs, SIMT, and Tensor Engines

- Lindholm, E., et al. (2008). NVIDIA Tesla: A unified graphics and computing architecture. *IEEE Micro*.
- Volkov, V. (2010). Better performance at lower occupancy. *GPU Tech Conf.*
- Markidis, S., et al. (2018). NVIDIA tensor cores. *IEEE IPDPSW*.
- Williams, S., et al. (2009). Roofline: An insightful visual performance model. *CACM*.

4. Models, Compilers, Scaling Laws

- LeCun, Y., Bengio, Y., & Hinton, G. (2015). Deep learning. *Nature*.
- Abadi, M., et al. (2016). TensorFlow. *OSDI*.

- Chen, T., et al. (2018). TVM: An automated end-to-end optimizing compiler. *OSDI*.
- Kaplan, J., et al. (2020). Scaling laws for neural language models. *arXiv:2001.08361*.
- Dao, T., et al. (2022). FlashAttention. *NeurIPS*.
- Pope, R., et al. (2023). PyTorch 2.0: TorchInductor. *PyTorch Dev Summit*.

5. Agents, Planning, Verification, Sandboxing

- Russell, S., & Norvig, P. (2021). *Artificial Intelligence: A Modern Approach* (4e).
- Kaelbling, L. P., & Lozano-Pérez, T. (2013). Integrated task and motion planning. *IJRR*.
- Dijkstra, E. W. (1976). *A Discipline of Programming*.
- Miller, M. S., et al. (2003). Capability-based security in E. *SECURITY*.
- Evans, D., et al. (1998). Proof-carrying code. *POPL*.

6. Multi-Agent Markets, Mechanism Design

- Milgrom, P. (2004). *Putting Auction Theory to Work*.
- Roth, A. E. (2015). *Who Gets What — and Why*.
- Nisan, N., et al. (2007). *Algorithmic Game Theory*.
- Roughgarden, T. (2016). *Twenty Lectures on Algorithmic Game Theory*.

7. Autonomic Systems, SRE, and Digital Twins

- Kephart, J. O., & Chess, D. M. (2003). The vision of autonomic computing. *Computer*.
- Beyer, B., et al. (2016/2020). *Site Reliability Engineering*; *The SRE Workbook*. O'Reilly.
- Bonomi, F., et al. (2012). Fog computing and its role in the IoT. *MCC Workshop*.
- Macal, C., & North, M. (2010). Tutorial on agent-based modeling. *J. Simul.*
- Camacho, E. F., & Bordons, C. (2007). *Model Predictive Control*.

8. Objective Layer: Proofs, Attestations, Privacy

- Leroy, X. (2009). Formal verification of a realistic compiler (CompCert). *CACM*.
- Klein, G., et al. (2009). seL4: Formal verification of an OS kernel. *SOSP*.
- NIST (2023). *AI Risk Management Framework (AI RMF 1.0)*.
- NIST (2020). *Zero Trust Architecture (SP 800-207)*.

- C2PA (2024). *Content Provenance & Authenticity Standard*.
- Dwork, C., & Roth, A. (2014). The algorithmic foundations of differential privacy. *Foundations and Trends*.
- Boneh, D., et al. (2020). Software transparency via Sigstore. *sigstore.dev* whitepaper.

9. Co-Designed Matter: Chiplets, Photonics, Packaging

- Sutherland, I., et al. (2019). *Logical Effort* (updated ed.). (cell sizing context).
- UCIe Consortium (2022–2024). *UCIe Specification*.
- Ayar Labs; Lightmatter; Lightelligence (2020–2024). Co-packaged optics whitepapers.
- Markov, I. L. (2014). Limits of CMOS scaling: A big picture. *CACM*.
- Kahng, A. B., & Mutlu, O. (2023). *Chiplets and the Future of IC Design*. Memos/ACM.
- ASML (2023–2025). High-NA EUV overview and system roadmaps (EXE series) technical notes.

10. Embodied Mesh: DTN, CRDTs, Safety Cases

- Cerf, V., et al. (2007). Delay-tolerant networking architecture (RFC 4838). *IETF*.
- Fall, K. (2003). A delay-tolerant network architecture. *SIGCOMM*.
- Shapiro, M., et al. (2011). A comprehensive study of CRDTs. *RR-7506, INRIA*.
- Kleppmann, M., & Beresford, A. (2017). A conflict-free replicated JSON datatype. *IEEE TKDE*.
- Ames, A. D., et al. (2019). Control barrier functions. *ECC/IEEE TAC*.
- Leveson, N. (2011). *Engineering a Safer World (STPA)*. MIT Press.
- ISO 26262 (2018/2022). *Road vehicles — Functional safety*.

Cross-Cutting Tooling, Benchmarks, and Governance

- MLCommons (2020–2025). *MLPerf* training & inference benchmarks.
- OpenTelemetry (2021–2025). *Tracing/metrics/logs specifications*.
- Open Policy Agent (OPA) (2019–2025). *Rego policy language & design*.
- OpenSSF (2021–2025). *SLSA Framework*; *Scorecards*; *Supply-chain security*.

Helpful Surveys and Overviews

- Sze, V., et al. (2017). Efficient processing of deep neural networks. *Proc. IEEE*.
- Jouppi, N. P., et al. (2017/2021). TPU architecture papers. *ISCA*.
- Narayanaswami, R., & Raghunathan, V. (eds.) (2022). *Embedded ML at the Edge*.
- Dean, J. (2021). Achieving rapid progress in AI. *Talk/notes*.